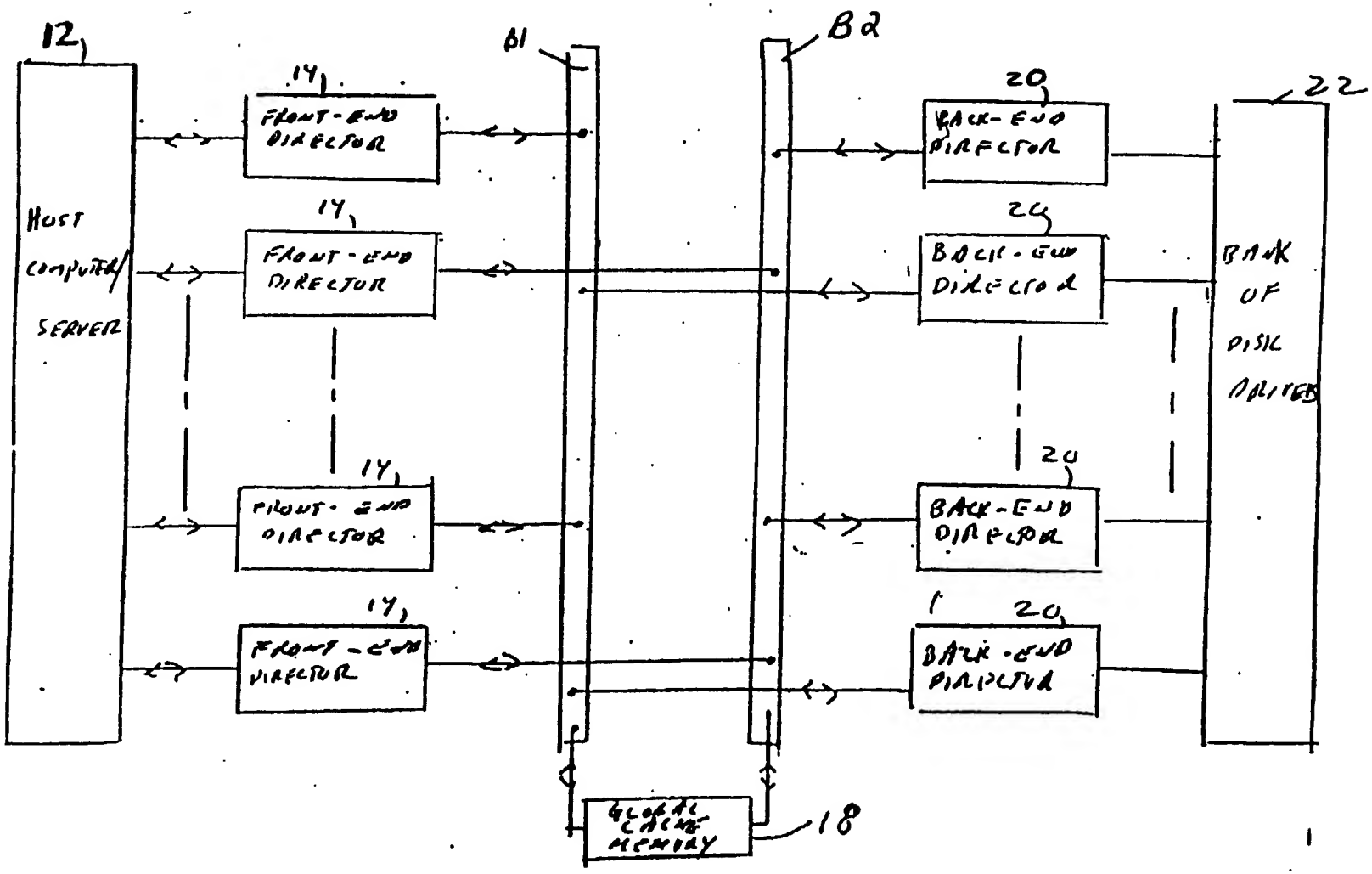
SCANNED, # 12

Christopher S. MacLellan et al.
METHOD FOR VALIDATING WRITE DATA
TO A MEMORY
Application No. 09/746,496

FIG. 1
PRIOR ART



SCANNED, # 12

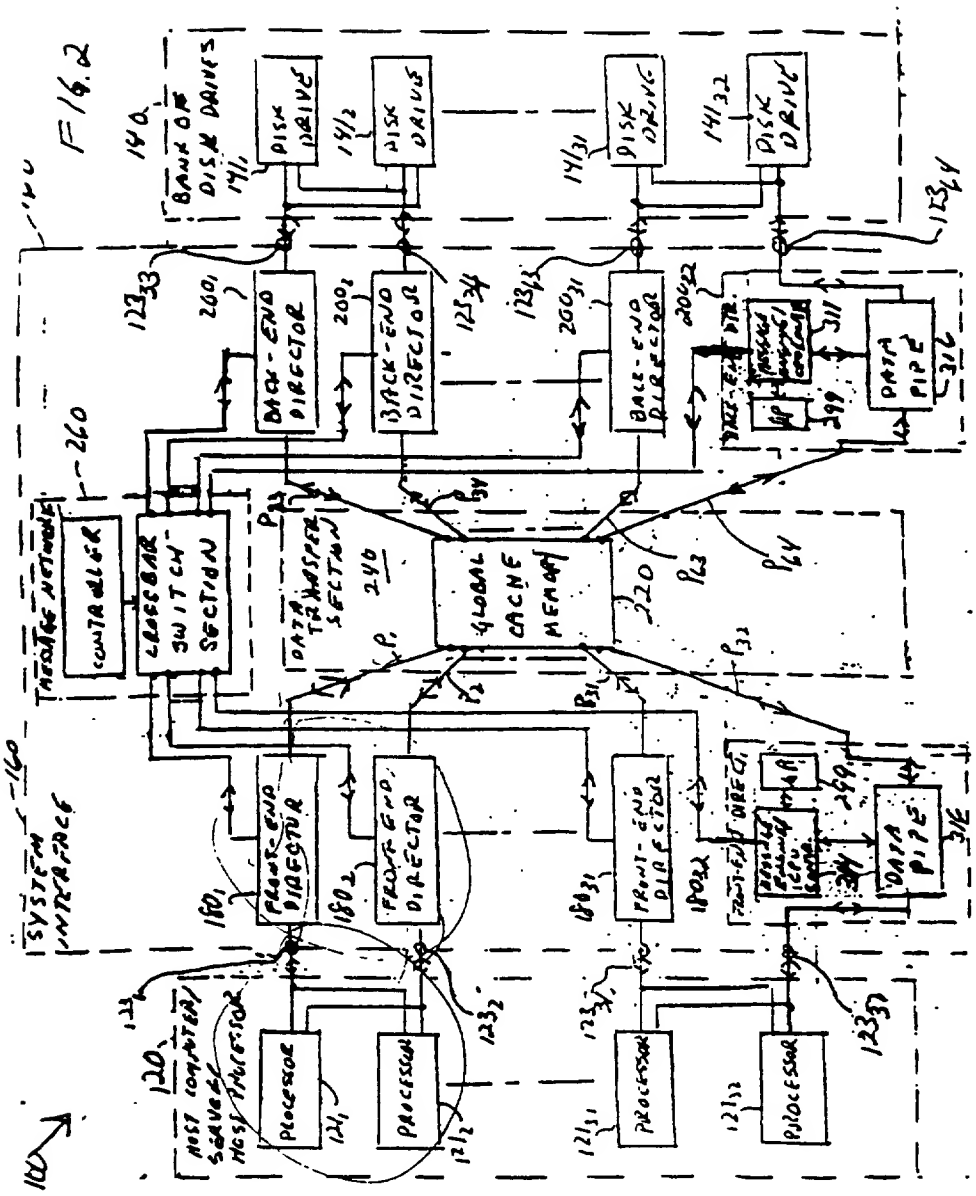


FIG. 2
100
120
140
160
180
200
220
240
260
300
310
312
320
DISK DRIVES
DISK DRIVE
BACK-END DIRECTOR
FRONT-END DIRECTOR
CROSSBAR SWITCH SECTION
GLOBAL CACHE MEMORY
DATA PIPE
PROCESSOR
SYSTEM INTERFACE

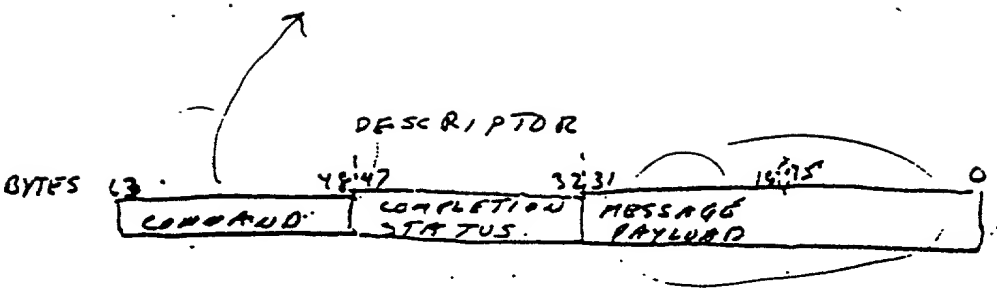

DESCRIPTOR
BYTES
63
48
47
32
31
16
15
0
COMMAND
COMPLETION STATUS
MESSAGE PAYLOAD

FIG 2A

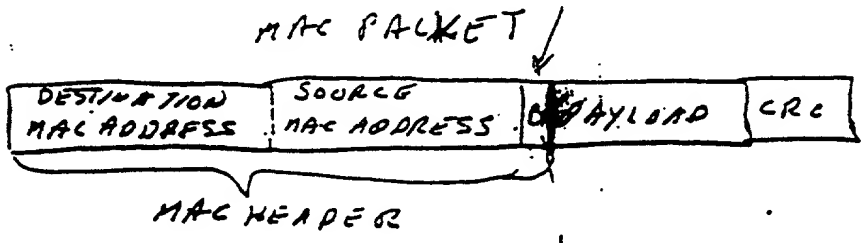

MAC PACKET
DESTINATION MAC ADDRESS
SOURCE MAC ADDRESS
PAYLOAD
CRC
MAC HEADER

FIG 2B

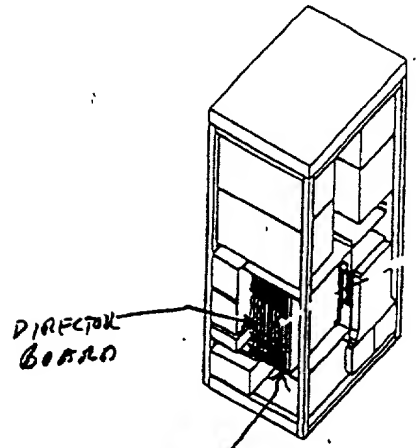
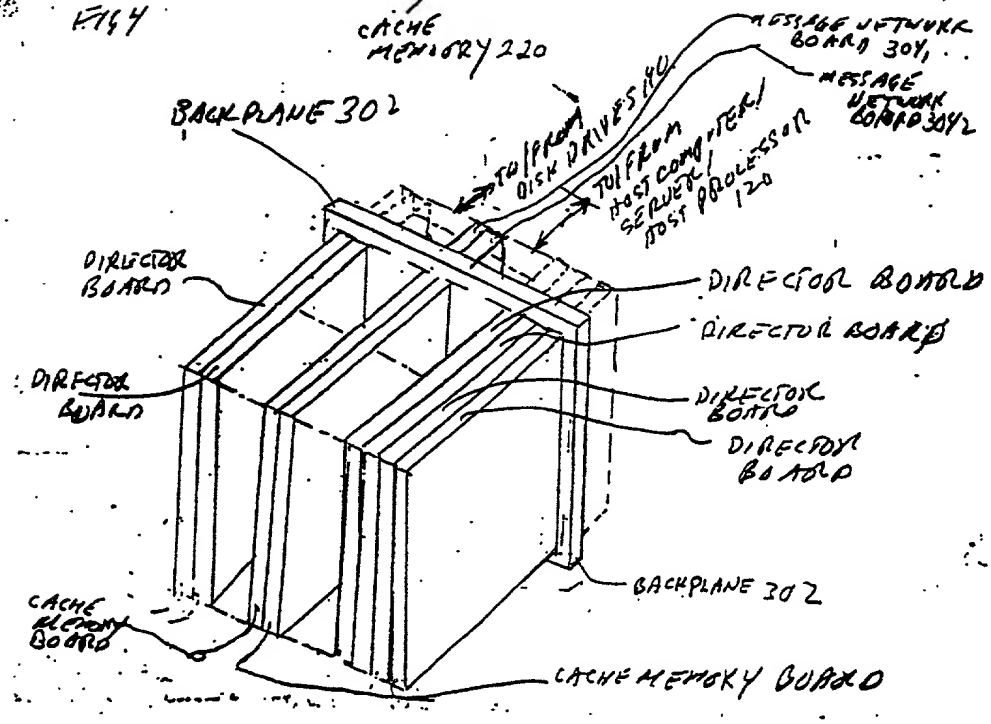
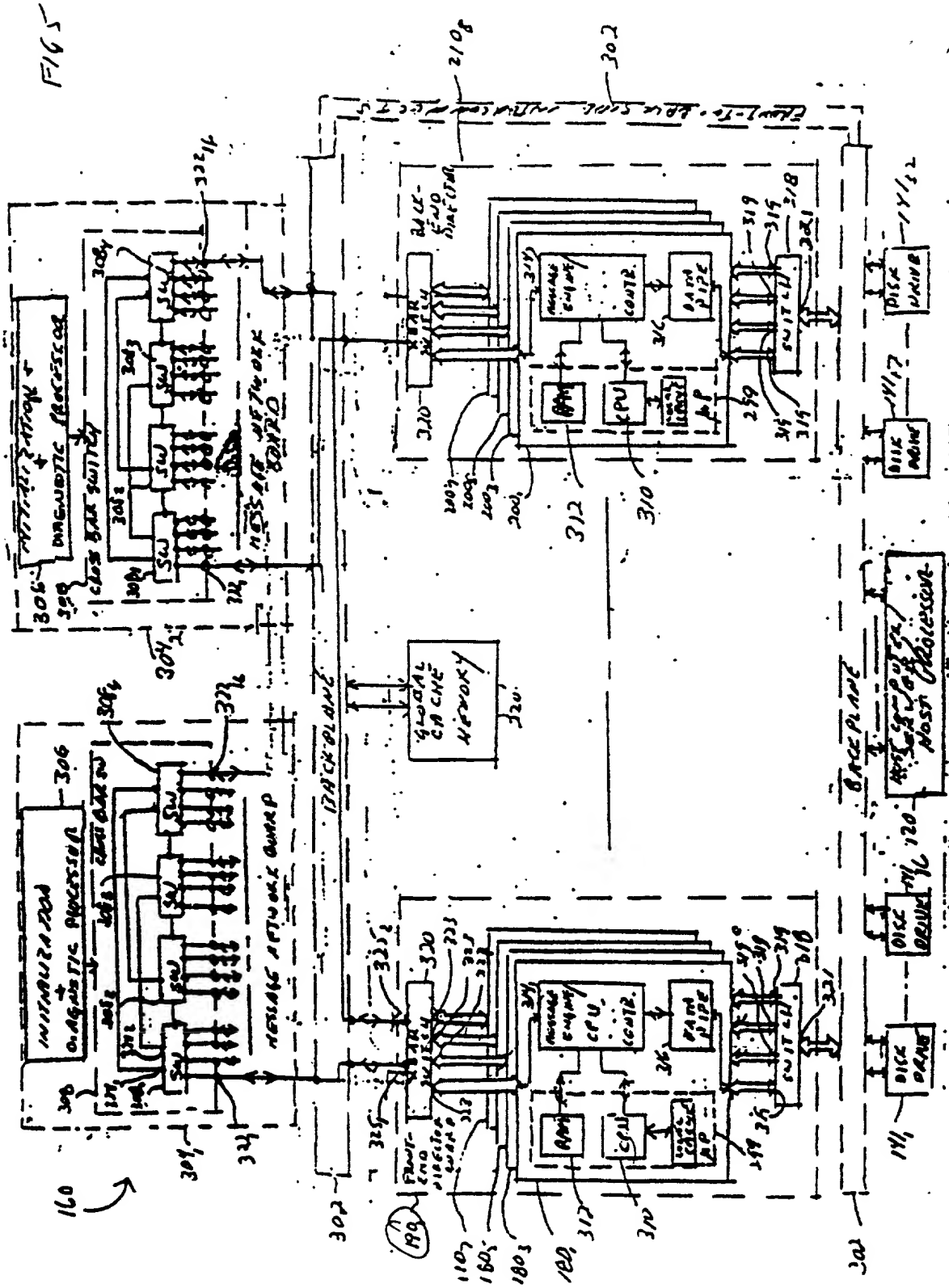
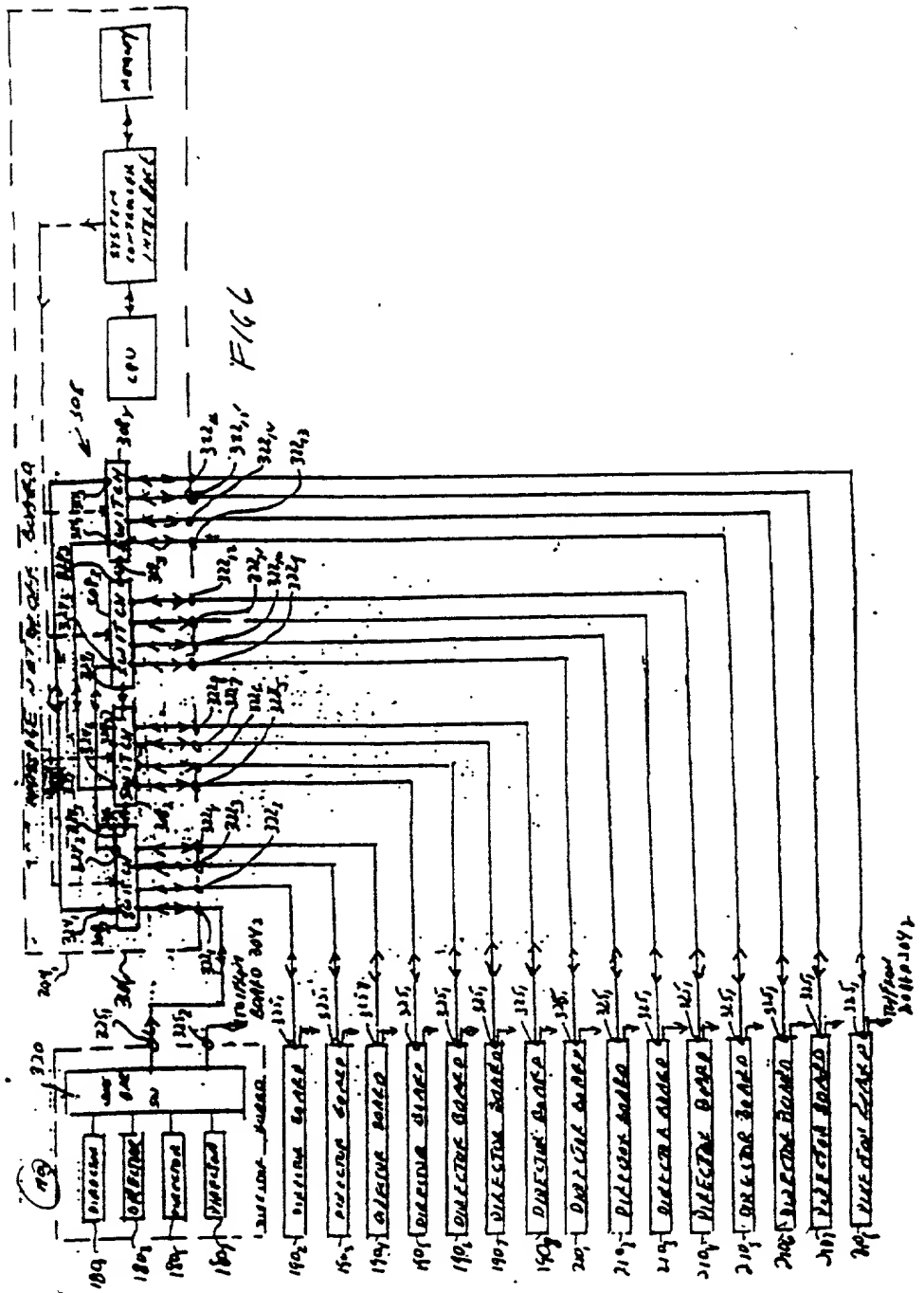

DIRECTOR BOARD
CACHE MEMORY 220

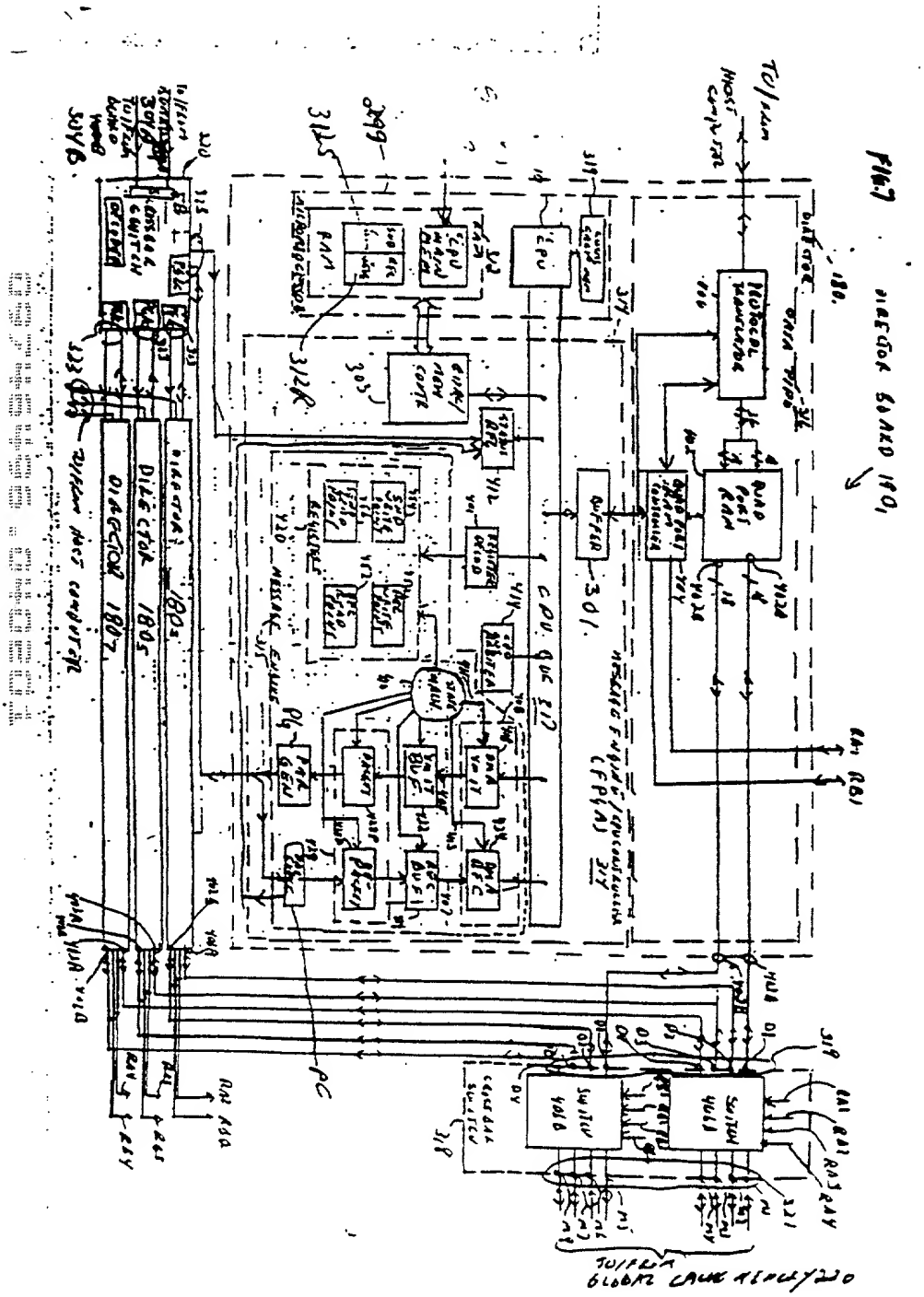
FIG. 4

FIG. 3


BACKPLANE 302
TO/FROM DISK DRIVES 140
TO/FROM HOST COMPUTER/ SERVER/ HOST PROCESSOR 120
MESSAGE NETWORK BOARD 304,
MESSAGE NETWORK BOARD 304,
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
DIRECTOR BOARD
BACKPLANE 302
CACHE MEMORY BOARD
CACHE MEMORY BOARD







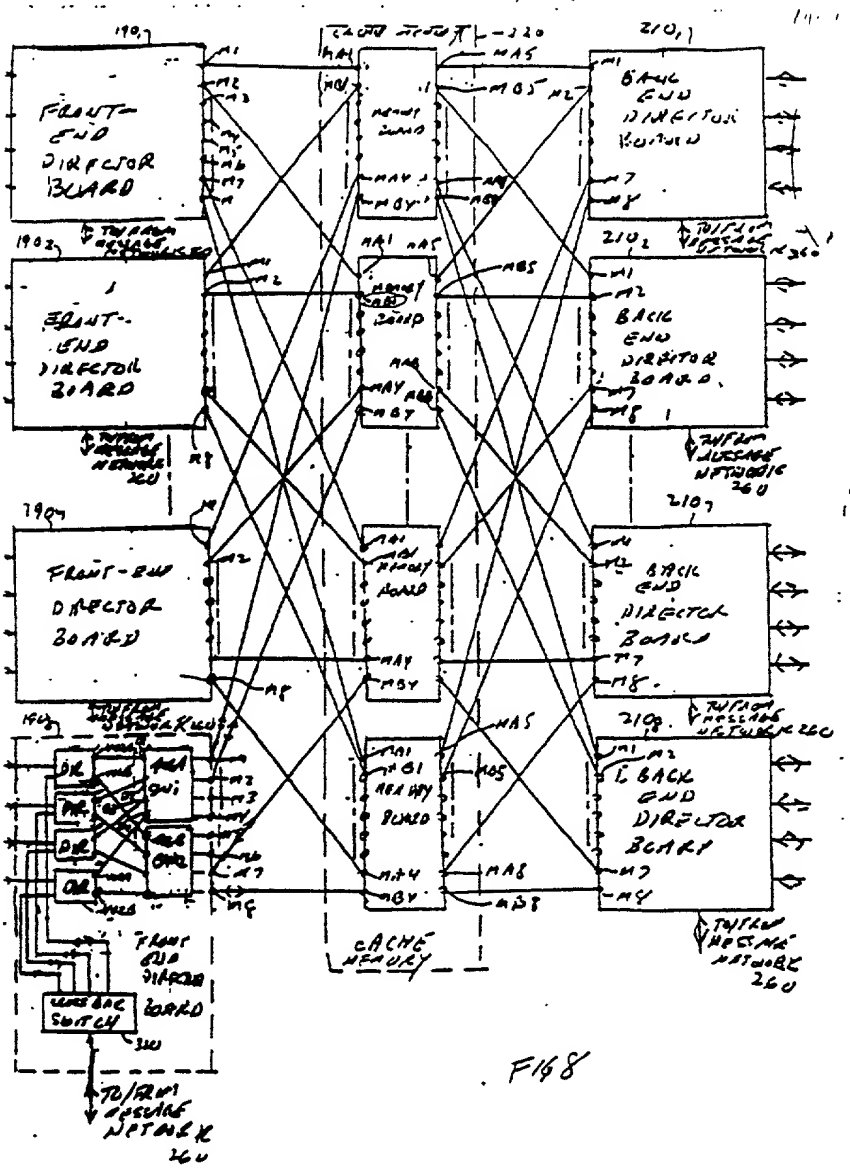

FRONT-END DIRECTOR BOARD
FRONT-END DIRECTOR BOARD
FRONT-END DIRECTOR BOARD
BACK END DIRECTOR BOARD
BACK END DIRECTOR BOARD
BACK END DIRECTOR BOARD
BACK END DIRECTOR BOARD
CACHE MEMORY
FRONT END DIRECTOR BOARD
SERVICE BUS SWITCH
TO/FROM SERVICE NETWORK 260

FIG 8

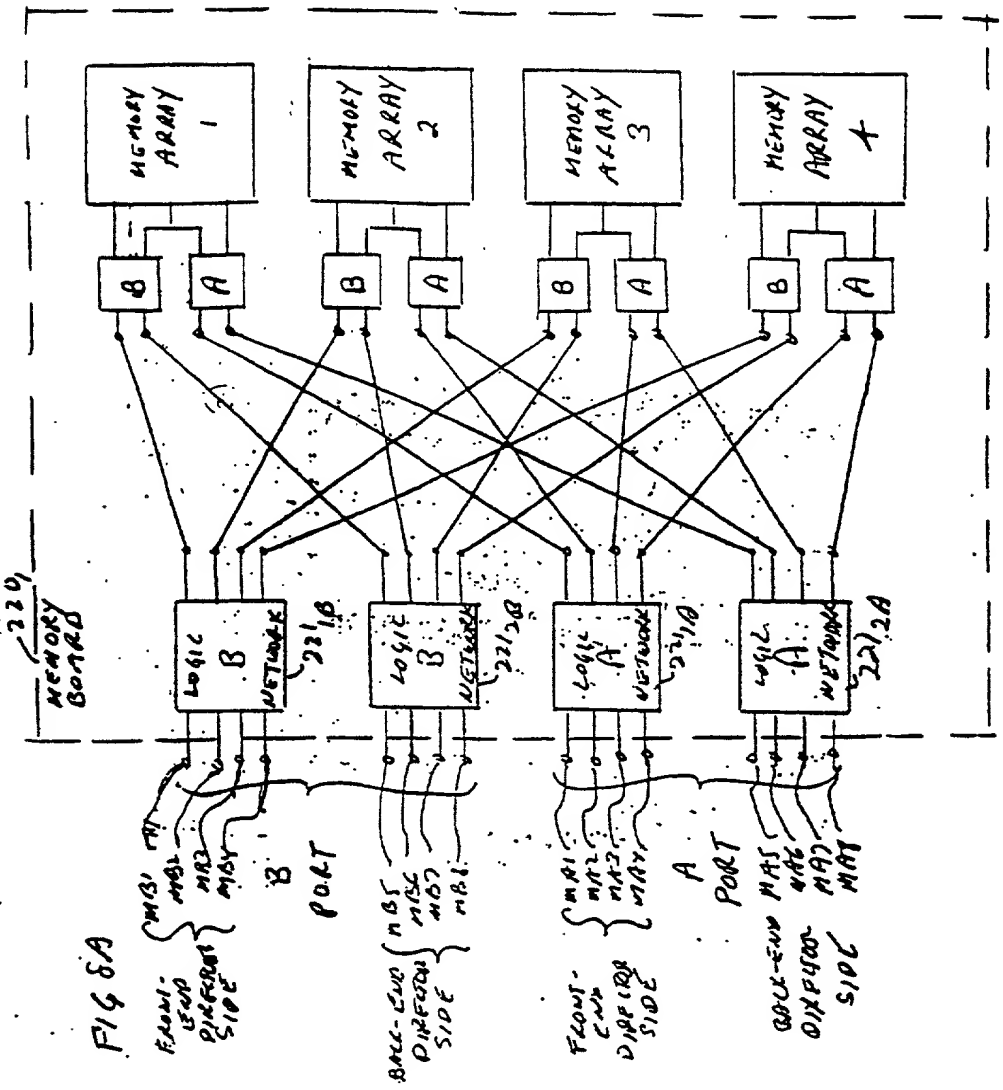

MEMORY ARRAY 1
MEMORY ARRAY 2
MEMORY ARRAY 3
MEMORY ARRAY 4
B
A
MEMORY BOARD
LOGIC NETWORK
B PORT
A PORT
FRONT-END DIRECTOR SIDE
BACK-END DIRECTOR SIDE

FIG 8A

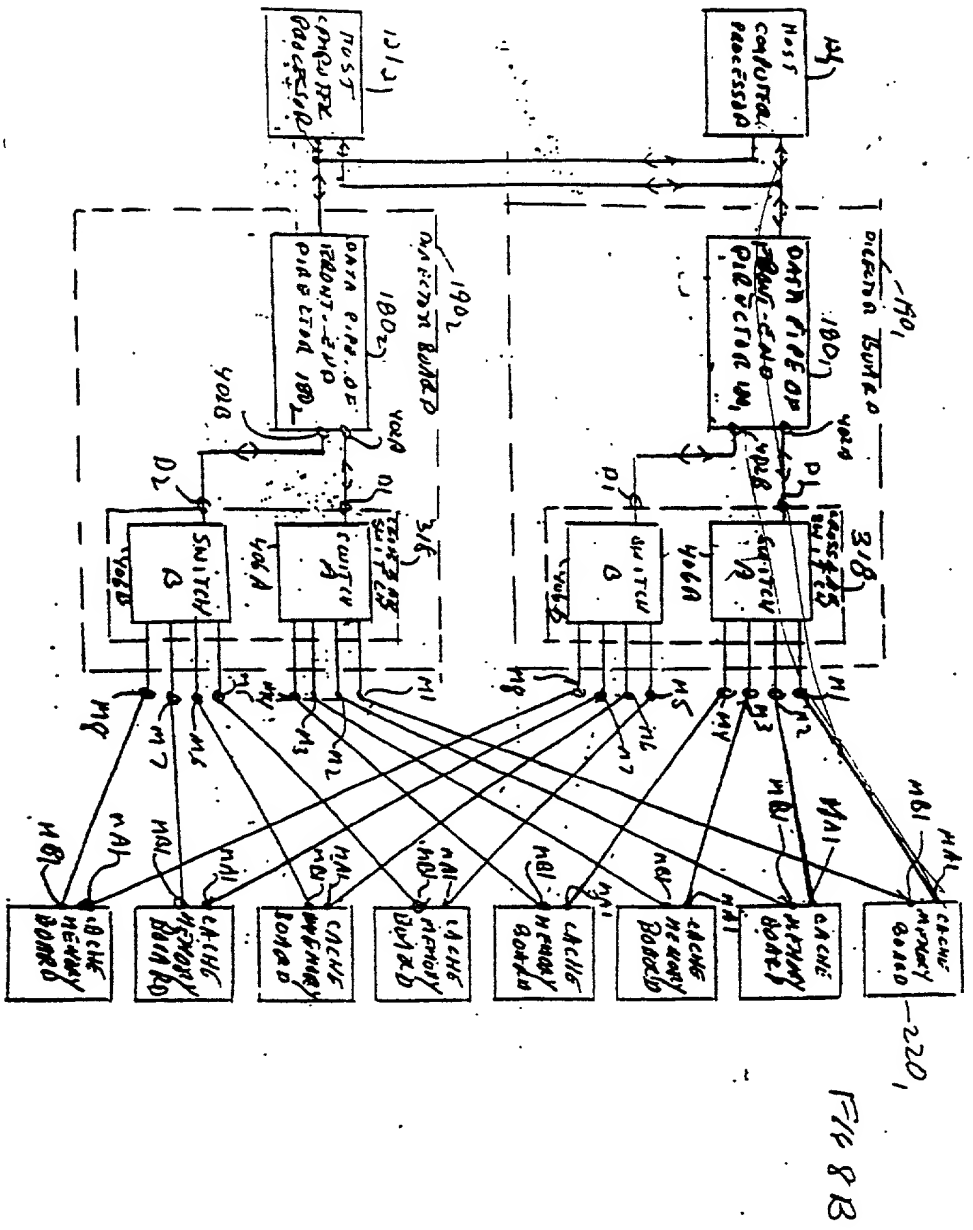


FIG 8B

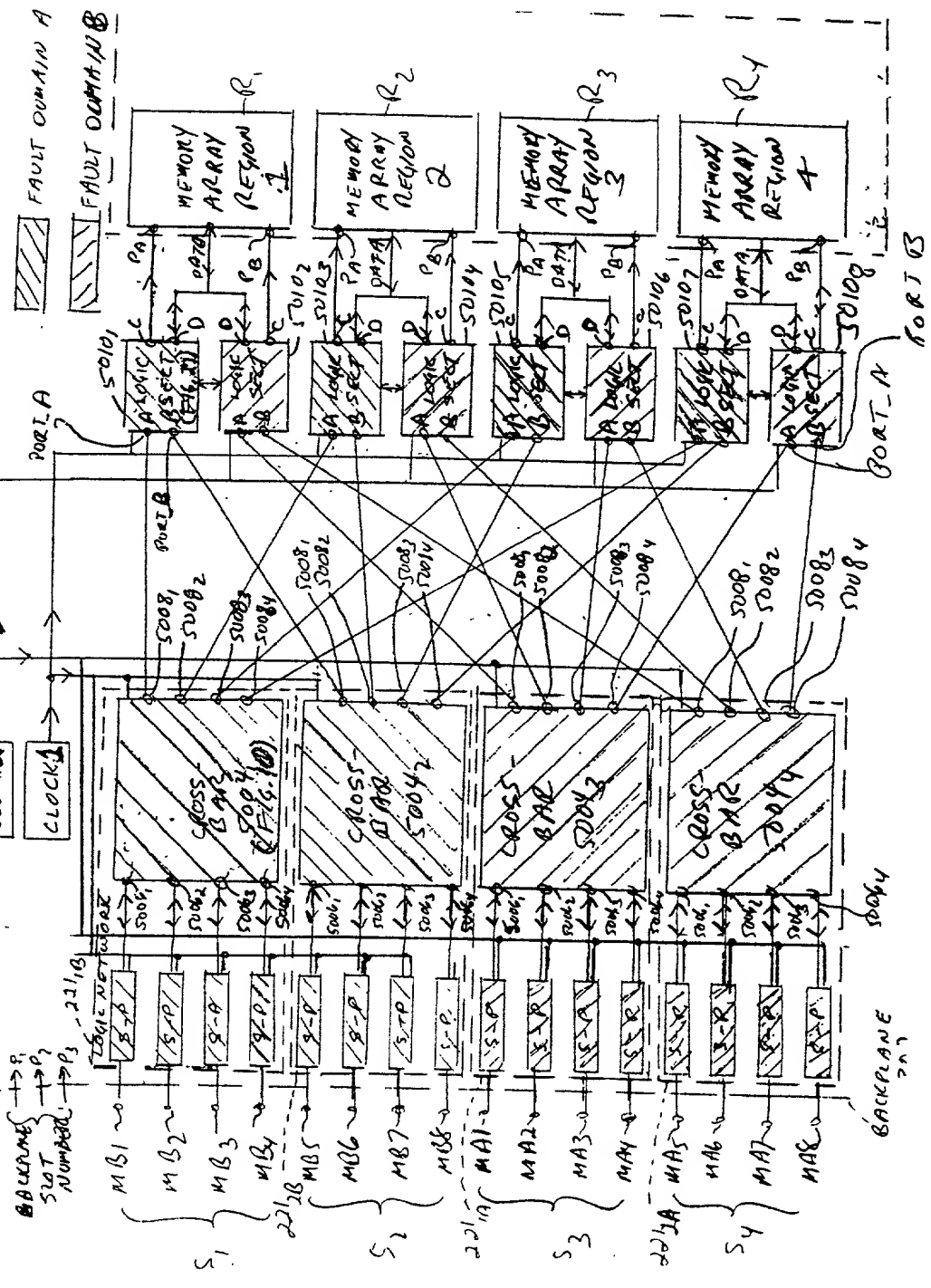

FAULT DOMAIN A
FAULT DOMAIN B
MEMORY ARRAY REGION 1
MEMORY ARRAY REGION 2
MEMORY ARRAY REGION 3
MEMORY ARRAY REGION 4
CLOCK 2
CLOCK 1
CROSS BAR SWITCH
BACKPLANE
PORT A
PORT B

FIG. 9

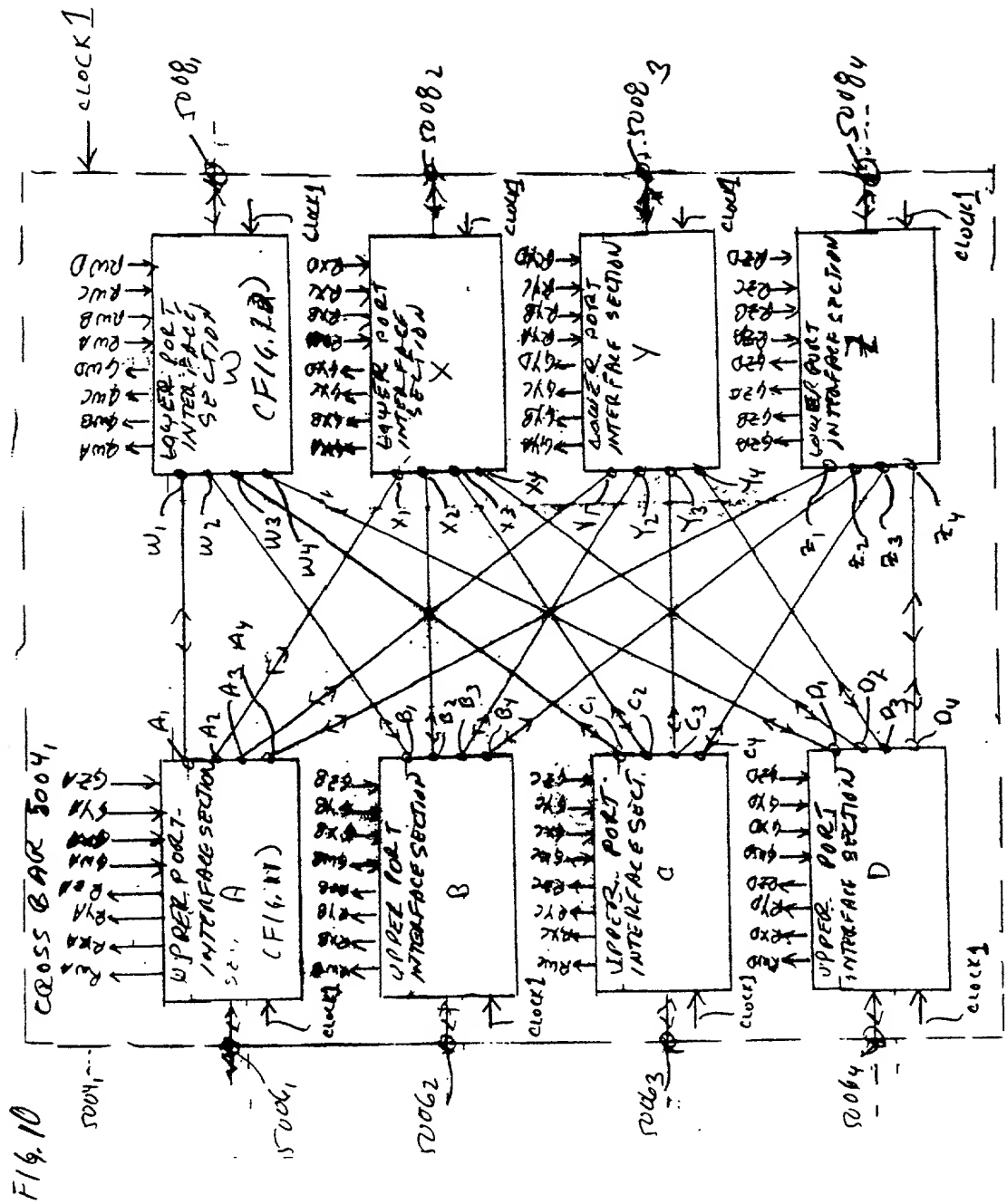

CLOCK 1
CROSS BAR SOC 4
LOWER PORT INTERFACE SECTION W (FIG. 12)
LOWER PORT INTERFACE SECTION X
LOWER PORT INTERFACE SECTION Y
LOWER PORT INTERFACE SECTION Z
UPPER PORT INTERFACE SECTION A (FIG. 11)
UPPER PORT INTERFACE SECTION B
UPPER PORT INTERFACE SECT. C
UPPER PORT INTERFACE SECTION D
SOC 1
SOC 2
SOC 3
SOC 4
CLOCK 1
CLOCK 2
CLOCK 3
CLOCK 4

FIG. 10

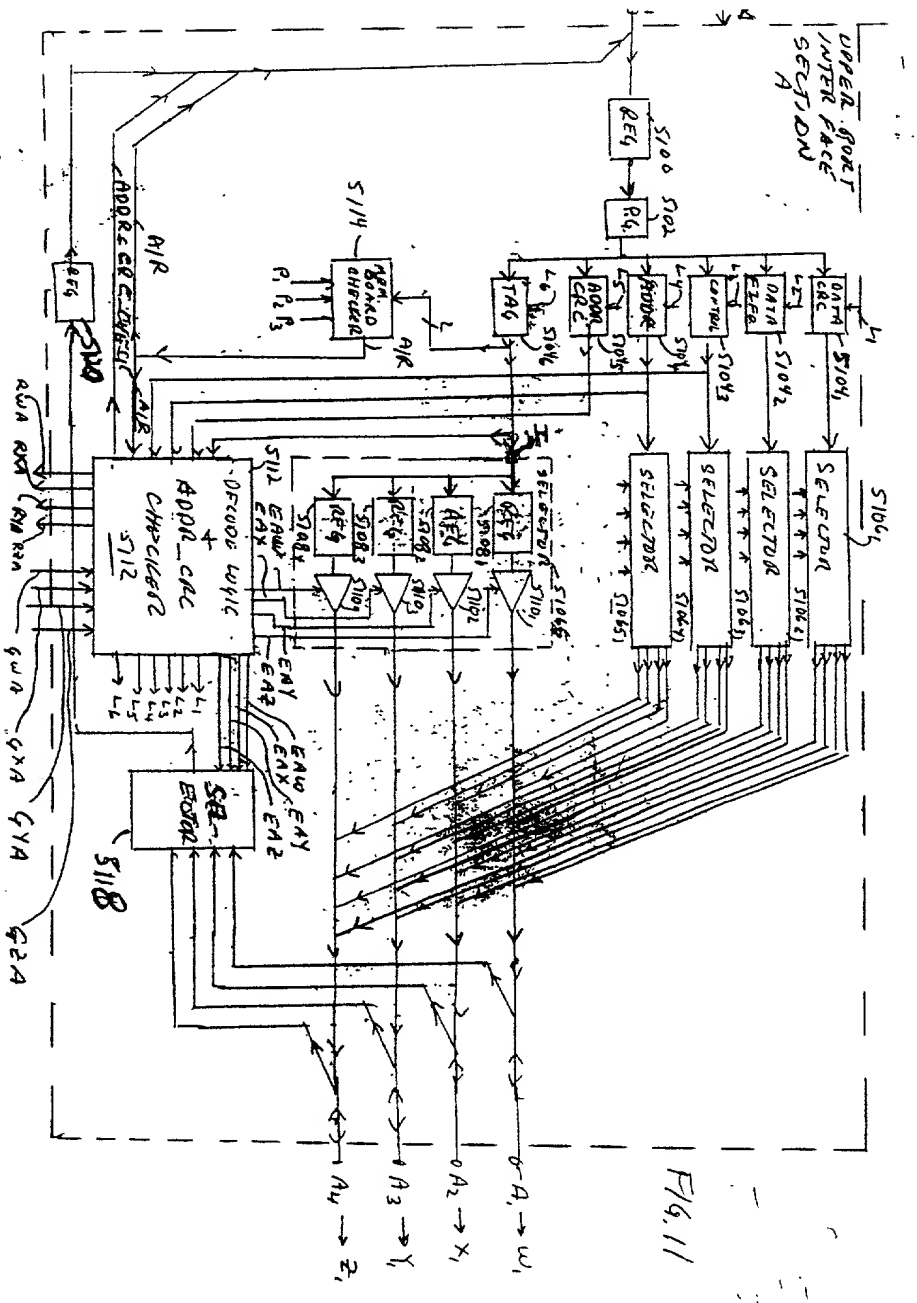

UPPER PORT INTERFACE SECTION
REG
RQ
ADDR
DATA
TAG
ADDR CRC
DATA CRC
SELECTOR
ADDR_CRC CHECKER
SEL
A/R
ADDR
DECODE LOGIC
A1
A2
A3
A4
A2 → X1
A3 → Y1
A4 → Z1

FIG. 11

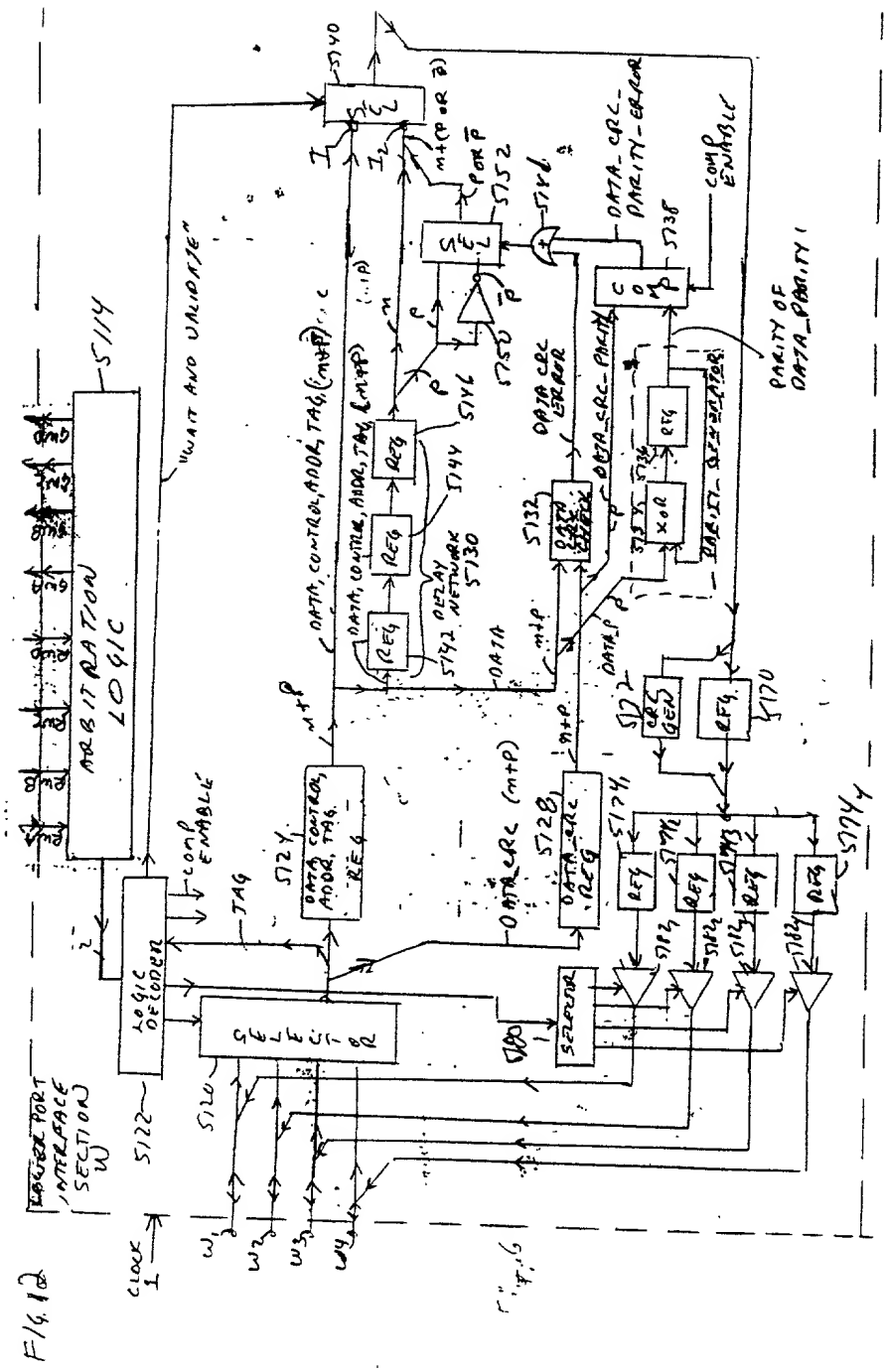

ARBITRATION LOGIC
WAIT AND UNLOAD
COMP ENABLE
TAG
DATA, CONTROL, ADDR, TAG
REG
DELAY NETWORK
DATA
DATA CRC ERROR
DATA_CRC_PARITY
DATA_PARITY_ERROR
COMP ENABLE
PARITY OF DATA_PARITY
LOGIC DECODER
SELECT
SEQUENCER
CRC GEN
XOR
COMP
EQ
CLOCK

FIG 1d

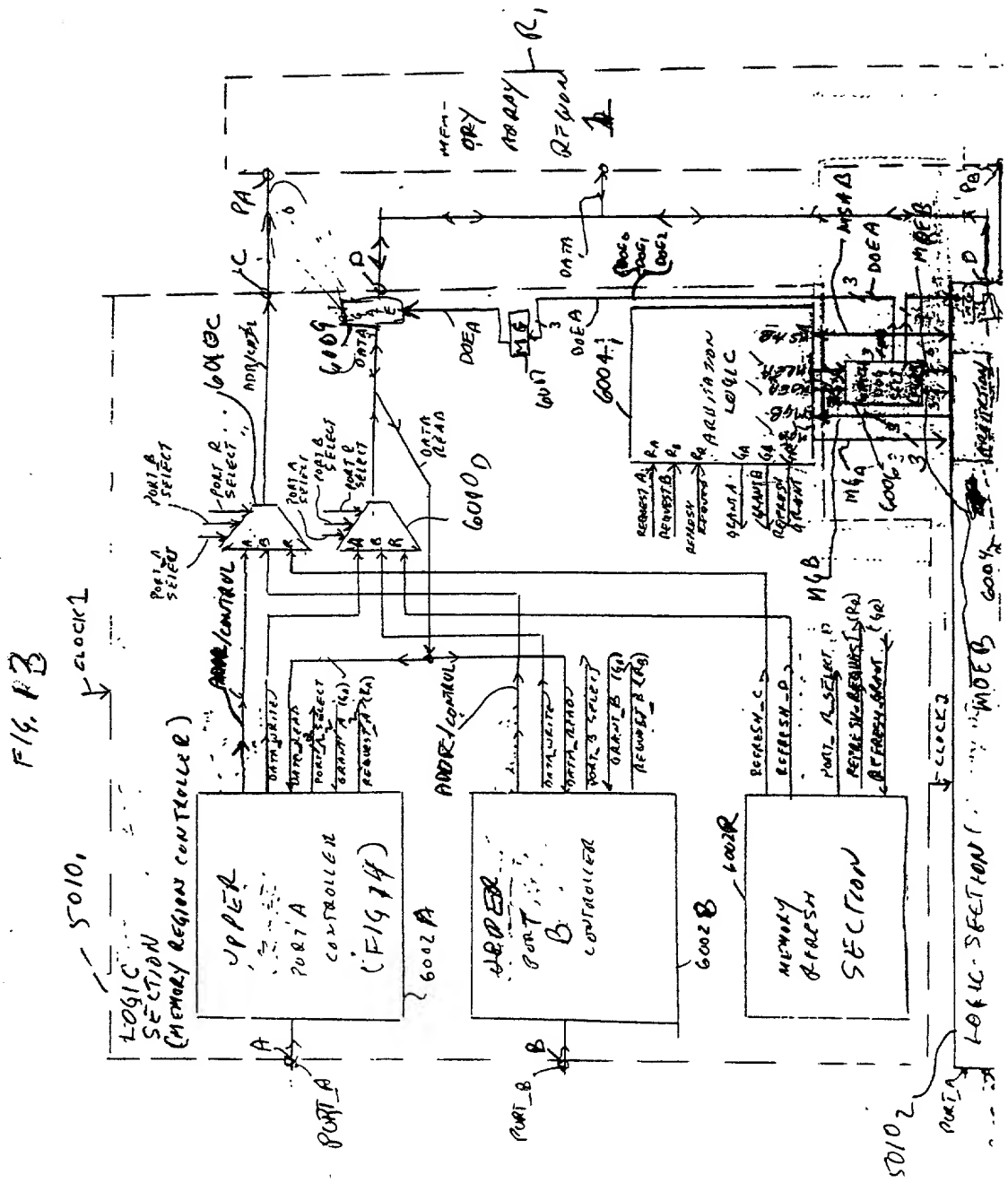
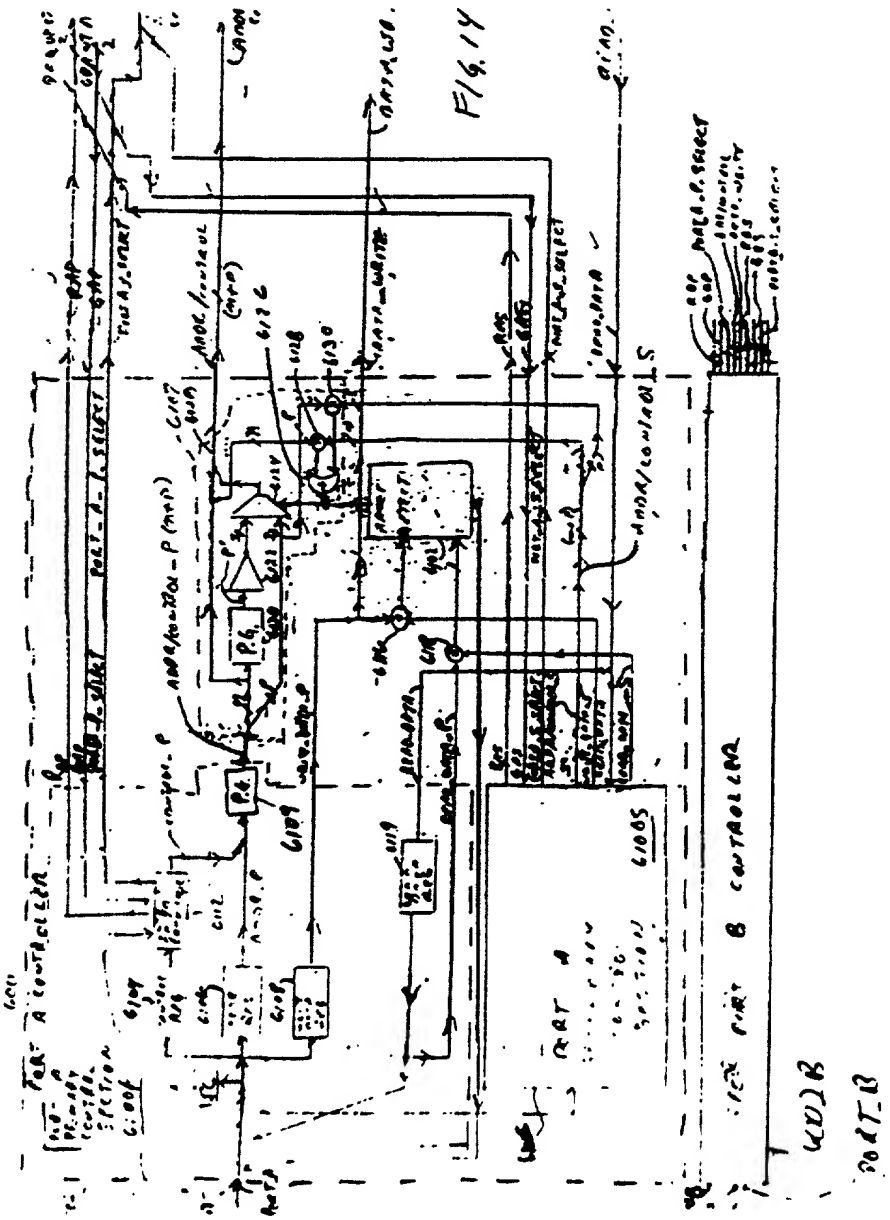
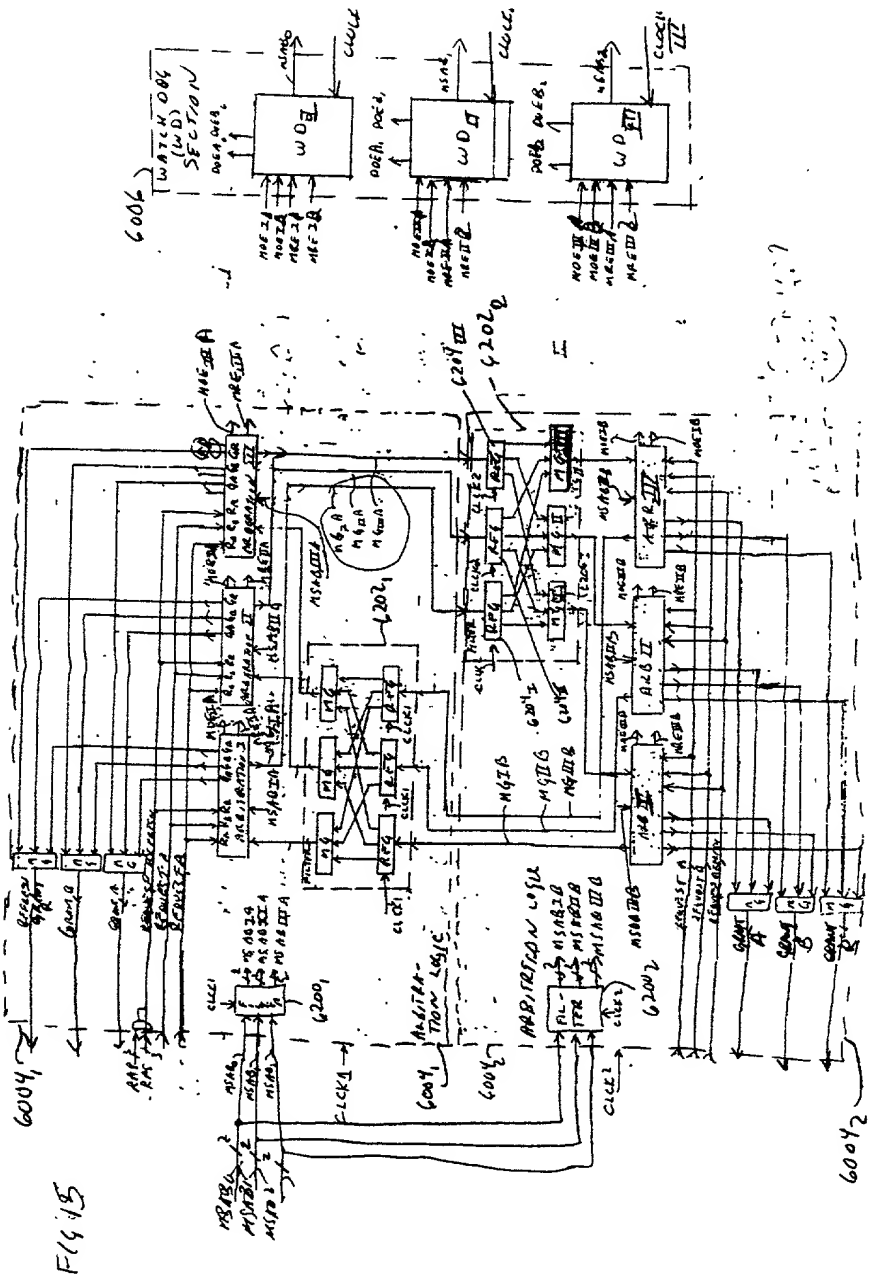
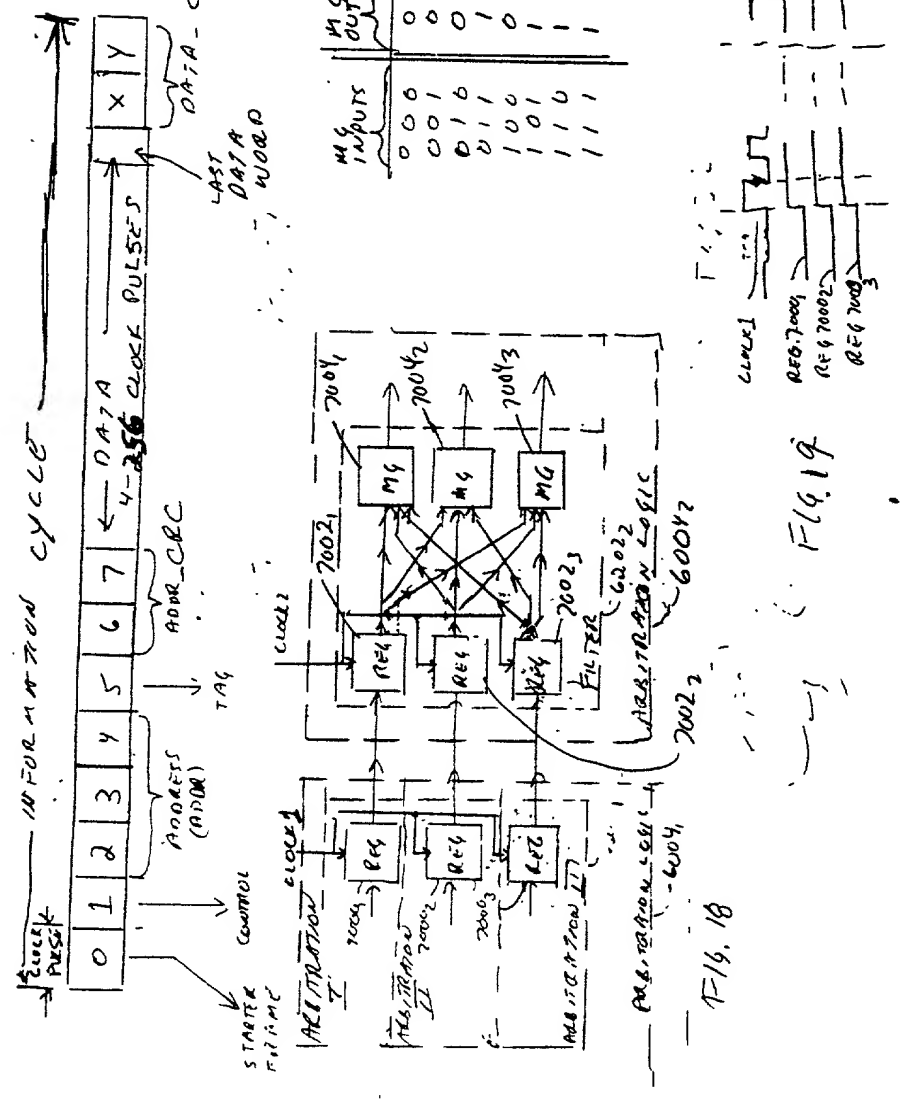
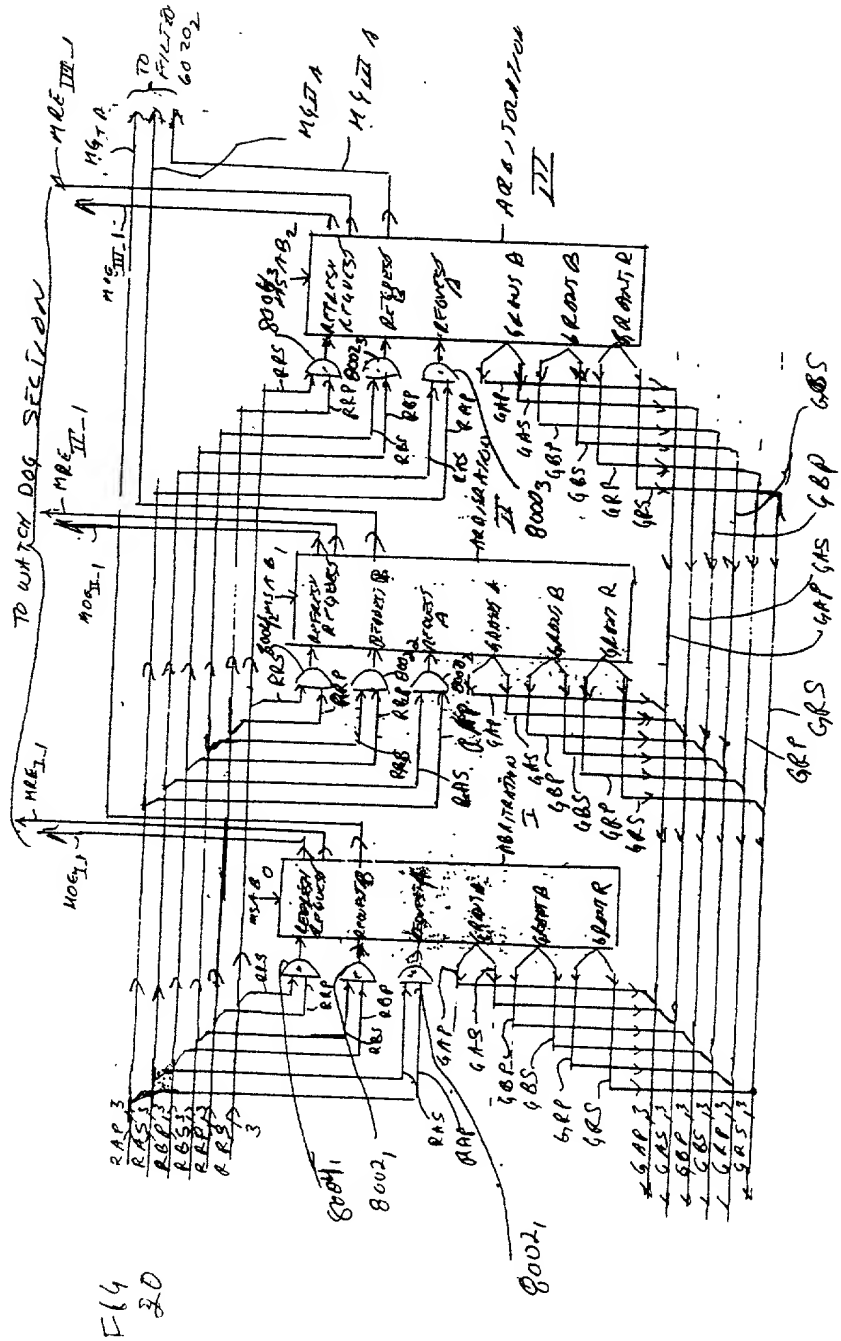


FIG. 13
LOGIC SECTION (MEMORY REGION CONTROLLER)
5010
CLOCK1
UPPER PORT A CONTROLLER (FIG 14)
6002A
LOWER PORT B CONTROLLER
6002B
MEMORY REFRESH SECTION
6002R
ADDR/CONTROL
DATA_WRITE
DATA_READ
PORT_A SELECT
REQUEST_A (RA)
REQUEST_B (RB)
REFRESH_C
REFRESH_D
PORT_A
PORT_B
CLOCK2
5010
LOGIC SECTION
PORT_A
MEMORY ARRAY
6004
6004-1
ARBITRATION LOGIC
6006
6008
6010
6012
DOE A
DOE B
MSEL A
MSEL B
MEA
MEB
MGA
MGB
REQUEST A
REQUEST B
GRANT A
GRANT B
REFRESH REQUEST
REFRESH GRANT






INFORMATION CYCLE
0
1
2
3
4
5
6
7
X
Y
ADDRESS (ADDR)
ADDR_CRC
4-256 CLOCK PULSES
DATA
DATA-CRC
LAST DATA WORD
FIG. 16
MS INPUTS
MS OUTPUT
MS OUTPUT
FIG. 17
REG
MS
FILTER
FIG. 18
FIG. 19
CLOCK 2


TO WATCH DOG SELECTOR
TO FILTER 60 202
ARB + TOKENIZER
ARB + TOKENIZER
ARB + TOKENIZER
80021
80021
80021